CLAIMS

We Claim:

1 A phase-locked loop, comprising:

a phase detector, a charge pump coupled to the phase detector, a low pass filter coupled to the charge pump, and a voltage control oscillator coupled to the charge pump and a supply voltage, wherein the low pass filter inputs a control voltage to the voltage controlled oscillator for generation of an output clock; and

a voltage regulator coupled to an output of the low pass filter, the voltage regulator for sensing the control voltage during normal operation of the phase-locked loop, and for dynamically adjusting the supply voltage in response to the control voltage, such that the phase-locked loop maintains the control voltage within a predefined range of a reference voltage.

2 The phase-locked loop of claim 1 wherein the voltage control regulator uses the control voltage as an error signal that is proportionate to process/temperature drift occurring in the phases locked loop.

3 The phase-locked loop of claim 2 wherein the voltage regulator comprises:

a summing node for continually sensing the control voltage and for comparing a combination of the control voltage and a current output of the self-adaptive voltage regulator to a reference voltage to determine an amount of drift occurring in the phase-locked loop;

a first loop gain for multiplying an output from the summing node to generate the supply voltage that is input to the voltage control oscillator; and

a second loop gain for multiplying the supply voltage by a continuation value to create a feedback voltage and for inputting the feedback voltage to the summing node as the current output of the voltage regulator,

wherein, in response to control voltage changes, the supply voltage is set such that the voltage control oscillator will cause the phase-locked loop to shift the control voltage towards the reference voltage, thereby compensating the phase-locked loop for temperature/process drift.

4 The regulator of claim 3 wherein the control voltage is input to the summing node through a first resistor.

5 The regulator of claim 4 wherein the second loop gain comprises second, third, and fourth resistors.

6 The regulator of claim 5 wherein the gain of the self-adaptive voltage control is altered by changing the values of the resistors.

7 The phase-locked loop of claim 6 wherein the phase-locked loop further includes:

a divider coupled between the voltage control oscillator and the phase detector for frequency multiplying the output clock up, thereby forming a first feedback loop.

8 The phase-locked loop of claim 7 wherein the voltage regulator forms a second feedback loop nested within the first feedback loop of the phase-locked loop.

9 A method for minimizing operational frequency limitations of a phase-locked loop, comprising:

(a) coupling an analog voltage regulator to the phase-locked loop, wherein the voltage regulator receives a control voltage from the phase-locked loop and outputs a supply voltage to a voltage control oscillator of the phase-locked loop;

(b) continually sensing the control voltage during normal operation of the phase-locked loop; and

(c) dynamically adjusting the supply voltage in response to the control voltage, such that the phase-locked loop maintains the control voltage within a predefined range of a reference voltage.

10 The method of claim 9 wherein step (c) further includes the step of: increasing the supply voltage when the control voltage is less than the reference voltage.

11 The method of claim 10 wherein step (c) further includes the step of: decreasing the supply voltage when the control voltage is greater than the reference voltage.

12 The method of claim 11 wherein step (b) further includes a step of:

(i) continually sensing the control voltage and the supply voltage; and

(ii) comparing the reference voltage to a weighted sum of the control voltage and the supply voltage to determine an amount of drift occurring in the phase-locked loop.

13 The method of claim 12 wherein the voltage control regulator uses the control voltage as an error signal that is proportionate to process/temperature drift occurring in the phases locked loop.

14 The method of claim 13 further including the step of implementing the phase-locked loop as a first feedback loop, and implementing the voltage regulator as a second feedback loop nested within the first feedback loop of the phase-locked loop.

15 A self-adaptive voltage regulator for use with a phase-locked loop, wherein the phase-locked loop includes phase detector, a charge pump coupled to the phase detector, a low pass filter coupled to the charge pump, and a voltage control oscillator coupled to the charge pump, wherein the low pass filter inputs a control voltage to a voltage controlled oscillator for generation of an output clock, the self-adaptive voltage regulator comprising:

a summing node for continually sensing the control voltage and for comparing a combination of the control voltage and a current output of the self-adaptive voltage regulator to a reference voltage to determine an amount of drift occurring in the phase-locked loop;

a first forward gain for multiplying an output from the summing node to generate a supply voltage that is input to the voltage control oscillator; and

a second feedback gain for multiplying the supply voltage by a continuation value and inputting the multiplied value to the summing node as the current output of the voltage regulator,

wherein, in response to control voltage changes, the supply voltage is set such that the voltage control oscillator will cause the phase-locked loop to shift the control voltage towards the reference voltage, thereby compensating the phase-locked loop for temperature/process drift.

16 The regulator of claim 15 wherein the control voltage is input to the summing node through a first resistor.

17 The regulator of claim 16 wherein the second loop gain comprises second, third, and fourth resistors.

18 The regulator of claim 17 wherein the gain of the self-adaptive voltage control is altered by changing the values of the resistors.